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Attorney's Docket No. 42P15685 PATENT
Confirmation No.: 6439

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Scott A. Hareland, et al.

Application No.: 10/607,769

Filed: June 27, 2003

For: Nonplanar Semiconductor Device with Partially or Fully Wrapped Around Gate Electrode and Methods of Fabrication

Examiner: Unassigned

Art Unit: 2812

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to MS: Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 14, 2006
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Dianne Neathery
(Typed or printed name of person mailing correspondence)

Dianne Neathery 2/14/06
(Signature of person mailing correspondence)

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

__X__ 37 C.F.R. §1.97(b).

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____ A statement pursuant to 37 C.F.R. §1.97(e) or

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(1) A statement pursuant to 37 C.F.R. §1.97(e); and

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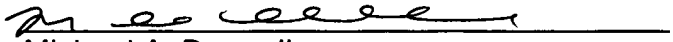
If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: February 14, 2006



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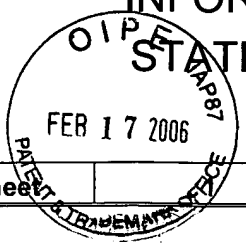

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Application Number	10/607,769
Filing Date	June 27, 2003
First Named Inventor:	Scott A. Hareland
Art Unit	2812
Examiner Name	Unassigned
Attorney Docket No.:	42P15685

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 2003/0098488 A1	05-29-2003	O'Keeffe et al.	
		US- 2003/0201458 A1	10-30-2003	Clark et al.	
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FOREIGN PATENT DOCUMENTS

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/607,769
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				Art Unit	2812
				Examiner Name	Unassigned
Sheet	**2**	**of**	**2**	Attorney Docket Number	42P15685

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		JING GUO, et al. "Performance Projections for Ballistic Carbon Nanotube Field-Effect Transistors", Applied Physics Letters, Vol. 80, No. 17, pp. 3192-3194 (April 29, 2004)	
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		DAVID M. FRIED, et al., "High-Performance P-Type Independent-Gate FinFETs, IEEE Electron Device Letters", Vol 25, No. 4, April 2004, pp. 199-201.	
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		CHARLES KUO, et al., "A Capacitorless Double-Gate DRAM Cell Design for High Density Applications", 2002 IEEE International Electron Devices Meeting Technical Digest, December 2002, pp. 843-846	
		TAKASHI OHSAWA, et al., "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1510-1522	
		T. TANAKA, et al., "Scalability Study on a Capacitorless 1T-DRAM: From Single-Gate PD-SOI to Double-Gate FinDRAM", 2004 IEEE International Electron Devices Meeting Technical Digest, December 2004, 4 pages.	L
		T. M. MAYER, et al., "Chemical Vapor Deposition of Fluoroalkylsilane Monolayer Films for Adhesion Control in Microelectromechanical Systems" 2000 American Vacuum Society B 18(5), Sep/Oct 2000, pp. 2433-2440	

Examiner Signature		Date Considered	

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